AMENDMENTS TO THE SPECIFICATION:

Amend the title to read: "Apparatus and Method for Recalibrating a Source-synchronoug Pipelined Self-Timed Bus Interface"

AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings of claims in the application.

LISTING OF CLAIMS:

What is claimed is:

Claim 1. (Currently Amended) In an SMP computer system having ~~an~~ a source-synchronous, pipelined, self-calibrating bus interface, the method of recalibrating the bus interface, comprising the steps of:

a) halting operations of said SMP computer system having ~~an~~ a source-synchronous, pipelined, self-calibrating bus interface with a system quiesce operation such that the bus interface is not used by the system, ~~to idle the interface,~~

b) fencing ~~the~~ a receiver of the bus interface,

c) recalibrating the bus interface using clock readjustment,

d) unfencing the receiver of the bus interface, and

e) taking the system of the bus interface out of the wait state and commencing operations to allow interface use again.

Claim 2. (Currently Amended) The method according to claim 1, wherein when said step of halting operations is done with a system quiesce operation to avoid using said bus interface to allow recalibrating of the bus interface during said system quiesce operation.

Claim 3. (Currently Amended) The method according to claim 1, wherein said step of calibrating the interface is accomplished by sending and sampling a known data pattern.

Claim 4. (Currently Amended) The method according to claim 1, wherein said step of calibrating the bus interface is accomplished by recalculating the frequency and applying the appropriate delay adjustment to the clock.

Claim 5. (Currently Amended) In an SMP computer system having ~~an~~ a source-synchronous bus interface, the method for re-calibration of the bus interface at periodic intervals comprising the steps of:

a. putting the system of the bus interface into a wait state with a system quiesce operation such that the bus interface is not used by the system,

b. performing a fast initialization process for calibration,

c. taking the system of the bus interface out of said wait state and restoring the system to a running state.

Claim 6. (Currently) The method according to claim 5 wherein wherein a step of data deskew has been performed as part of the original system bus interface initialization, and during recalibration of only a single clock centering step for the bus interface is performed during said fast initialization process for calibration without deskewing data during said fast initialization step performed for re-calibration.

Claim 7. (Currently Amended) The method according to claim 6 wherein said wait state keeps the bus interface from being used for processing steps other than re-calibration and sending a calibration pattern and allowing ~~claibration~~ calibration logic to re-center the clock applicable to the bus interface to compensate for new environmental conditions and circuit changes.

Claim 8. (Currently Amended) The method according to claim 7 wherein the recalibration of the bus interface is triggered periodically and in a ~~mannter~~ manner that circuit or environmental characteristics over time do not adversely affect the operation of the bus interface.

Claim 9. (Currently Amended) The method according to claim 7 wherein the re-calibration is based on a trigger event which triggers the steps for re-calibration of the bus interface

Claim 10. (Currently Amended) The method according to claim 1 ~~whrein~~ wherein a quiesce of the system of the bus interface if performed prior to performing a fast initialization process for calibration, and during calibration, the step of calibrating the bus interface recalculates the frequency of the clock for the bus interface and applies an appropriate delay adjustment to the clock for the bus interface, after which the system for the interface is unquiesced before commencing operations to allow bus interface use again.

Claim 11. (Currently amended) The method according to claim 10 wherein the recalibration ~~stem~~ step includes sending a pattern across the interface and adjusting the clock through re-centering without data de-skewing but with ~~shifing~~ shifting to the clock to re-center the ~~intrface~~ bus interface data capturing window for the 'eye' of the data capturing window.

Claim 12. (Currently Amended) The method according to claim 10 wherein the recalibration stem includes re-calculating the clock frequency of the bus interface against the current hardware and re-applying the clock frequency calculation to

the clock delay to re-center the clock when the machine is being cycled down to failure and the major change needing re-calibration is cycle time.

Claim 13. (Currently Amended) The method of claim 5 wherein a state machine controls calibration, and said state machine allows

a. putting the system of the interface into a wait state and for quiescing the data over the bus interface when the state machine enters a re-calibration state, whereupon,

b. said a fast initialization process for calibration is performed, and then

c. a change of said ~~stae~~ state machine ~~changes~~ takes the system of the bus interface back out of said wait state; and

d. ~~Allows~~ allows data to transfer across the bus interface again.